

~~7~~ 65. (New) The circuit of claim ~~59~~<sup>1</sup>, further comprising an analog-to-digital converter coupled to outputs of the inverting and non-inverting circuits for generating a digital signal based upon the outputs.

*sub D1* ~~8~~ 66. (New) The circuit of claim ~~65~~<sup>7</sup>, wherein the control circuit monitors the digital signal and applies the control signals to the switching devices to maintain the digital signal within a desired range.

*Control* ~~9~~ 67. (New) The circuit of claim ~~59~~<sup>1</sup>, wherein the input resistance of the inverting circuit is a fixed resistance.

~~10~~ 68. (New) The circuit of claim ~~59~~<sup>1</sup>, wherein the feedback resistance of the non-inverting circuit is a fixed resistance.

~~11~~ 69. (New) The circuit of claim ~~59~~<sup>1</sup>, wherein the feedback resistance circuit is configured to selectively place the plurality of first resistances in parallel with one another, and the input resistance circuit is configured to selectively place the plurality of second resistances in series with one another.

#### REMARKS

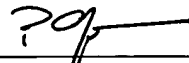
Prior to the present Preliminary Amendment, claim 1 was pending in the present Application. By this paper, claim 1 is canceled without prejudice and new claims 32-69 have been added. Upon entry of this Amendment, claims 32-69 will be pending in the present Application.

The new claims have been added to provide alternative scope and to more clearly and distinctly point out aspects of the invention.

If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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